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www.entiv.com

WHITE PAPER

THE ADVANTAGES OF A FRONT-TO-BACK FLOW FOR WINDOWS-BASED PCB DESIGN

[1]BACKGROUND

As electronic systems increase in complexity, geometries continue to shrink, and market introduction times grow ever more critical, the PCB designer has little room for error – or much time to breathe. Designers need to move from schematic capture to simulation to layout and routing, and back again, as efficiently and skillfully as possible
Without any miscues along the way. They need tools that will help them make informed decisions as they work,
Without having to leave the design environment.
This paper will explore the need for an integrated suite of PCB design and layout tools and will show how Orcad
Unison Suite meets that need. We will examine the function of each tool and how its tight integration with the
Orcad Unison Suite helps to speed design along.

THE ORCAD UNISON SUITE FOR PCB DESIGNERS AND ENGINEERS TASKED WITH MORE

In the past, design teams used loosely connected tools to capture circuit designs in schematic form and then to
simulate them. Designs were thrown over the wall to teams of layout designers to determine optimum placement of
circuit components and optimum routing of the connectors. Very often, designers and layout engineers spent a large portion of their time translating component files, manually resynchronizing data, and dealing with design integrity problems due to the lack of integration between the capture, simulation and layout tools they were using.
During the last decade, designers began to combine analog, digital and even RF components onto the same board.
Geometries shrank, time to market pressures shortened design cycles, and the need arose for more integrated
capture, simulation and layout tools. Budget constraints and the need for easy-to-learn, easy-to-use tools gave rise to the need for low cost solutions with broad capabilities. Where designs had once been passed off from one team to another, now a single design team – sometimes a single individual – is required to take a design from conception to manufacturing drawings. Out of necessity, designers and engineers are being tasked with more.
Most problems in PCB designs can be traced to incorrect component information or poor communication between
designer and layout tools. The tight integration of the Orcad Unison Suite eliminates these sources of errors and
allows the designer to move board designs from creation to manufacturing with more complete information every
step of the way.

THE TYPICAL DESIGN WORKFLOW

The typical PCB design workflow includes: creating an electronic circuit, simulating the design, creating the board

layout, routing the board, generating the manufacturing output, and maintaining the design through ECO cycles.

1

CIRCUIT DESIGN WITH ORCAD CAPTURE

Circuit design involves placing and connecting parts on a schematic, specifying how they are to be packaged, uniquely identifying them, adding information for simulation and board layout, and incorporating information from
external functions. Typically this is an iterative process where one section of circuitry is defined and evaluated, then redefined and re-evaluated. Tight integration between Orcad Capture and PSpice enables this iterative process, allowing the designer to verify proper circuit operation before moving forward.
Orcad Capture's Project Wizard assists in new circuit design and smoothes communication with PSpice and Orcad
Layout. Creating a new project based on an existing Analog or Mixed A/D project, or by using of one of the provided template projects ensures that the project includes all required PSpice elements such as simulation profiles and configured PSpice libraries.

Two workspace preferences set in Orcad Capture further aid the use of PSpice and Orcad Layout.

o Auto Reference speeds design entry for sections of the design to be simulated with PSpice.
o Intertool Communication allows cross probing between Orcad Capture and PSpice when designing the circuit, and between Orcad Capture and Orcad Layout when working on the board layout.

Placing parts and making wire connections between them populates the design. To speed the design process, Orcad Capture allows the designer to import part or all of another design by transferring its schematic folders or schematic pages or by copying and pasting sections of schematic pages.
Parts and nets are described by properties, which consist of a name and value. Orcad Capture's Property Editor
allows the designer to set property values that pass information to the PSpice simulation to assist in the board
layout. The Property Editor's PSpice filter narrows the scope of displayed properties to those that are significant for
PSpice simulation. The Property Editor's Layout Filter narrows the scope of displayed properties to those needed for reviewing and editing board layout properties. Capture also allows designers to export out all the part or net
properties to EXCEL spreadsheet and import back with all the changes.
A simulation profile, which defines the type of simulation to be performed and the resources to be used in the
simulation, must be created before a PSpice simulation can be run. Simulation profiles can be edited in Orcad
Capture with the Edit Simulation Profile command in the PSpice menu. In PSpice, the Edit Profile command in the
Simulation menu provides the same functionality.
With the simulation profile defined, the simulation can be launched from Orcad Capture. This automatically performs an Electrical Rule Check (DRC), generates a netlist, launches PSpice, and passes the netlist and simulation settings to PSpice. PSpice then performs the circuit analysis on the design and can even display signals of interest automatically.

[2]SIMULATING WITH PSPICE A/D BASICS

PSpice A/D Basics is closely integrated with Capture to provide a rapid design-and-simulate iterative cycle. It allows various design configurations to be explored before committing to a specific implementation. PSpice is a fullfeatured analog and mixed-signal simulator that performs DC sweep, AC sweep, transient, noise, Fourier, and
temperature analyses. It includes a rich set of mathematical functions that can be applied to simulation output to
provide measurement values or waveforms. With Orcad Capture and PSpice A/D Basics, the designer can create
designs, control simulations, and interpret the results within a single environment.
Using Orcad Capture, the designer sets up and runs simulations using graphical dialogs. During simulation, the
progress of the simulation appears and is updated in the PSpice simulation output window. PSpice creates an output file containing bias point information that can be displayed on the circuit schematic in Orcad

Capture, and another file containing waveform data for displaying the simulation results in PSpice's Probe window.
After completing the simulation, PSpice plots waveform results so the designer can visualize circuit behavior and
determine design validity. Graphical results of each simulation are presented in PSpice's Probe window waveform
viewer and analyzer. By default, PSpice displays simple voltages, currents, and noise data from the circuit simulation.
Using PSpice's Trace menu, users can display simple voltages and currents, display complex arithmetic expressions of those signals, or even look at Fourier transforms of voltages and currents.
Orcad Capture displays bias voltage and current information on the circuit schematic to help with the analysis. The
designer can cross-probe simulation results by adding markers to the desired pins and nets in the circuit schematic. Markers indicate the points for which the designer would like to see simulation waveforms displayed in PSpice.
2
Placing these markers in the schematic is the equivalent of placing an oscilloscope probe on a point in a circuit
breadboard. Performing a PSpice simulation corresponds to building or changing a breadboard; performing waveform analysis corresponds to looking at the breadboard with an oscilloscope.
The Markers submenu in Orcad Capture provides options for controlling the display of marked results in PSpice. For mixed analog/digital simulations, analog and digital waveforms are displayed simultaneously with a common time base.
Multiple simulation profiles can be created and saved for later recall and comparison. For longer simulations, realtime "marching waveforms" can be viewed as the simulation progresses. Or, other designs can be edited while long simulations are running in the background.
PSpice calculations and results are reported in the simulation output file and provide an audit trail of the simulation
if results are not as expected. Taken together, simulation and waveform analysis is an iterative process. After analyzing simulation results, you can refine your design and simulation settings, then perform new simulation and
waveform analyses.

COMPLETING THE DESIGN AND MOVING TO LAYOUT

After completing the iterative design-simulate process, Orcad Capture helps the designer prepare the design for
layout with the following tools:
o The Annotation Tool makes sure that all parts in the design have a unique reference designator. It assigns unique alphanumeric part references, and assigns individual parts to the various elements of multiple-part packages.
o The Design Rules Check scans the schematic folders to make sure there are no unconnected parts, unwanted
connections, or other invalid conditions; then, it generates a report and places markers on problem spots.
o The Bill of Materials Report is a list of all the elements needed for the board design. It can be a tab-delimited part
list or a custom bill of materials showing designer-specified properties.
o The Cross Reference Tool creates a report, indexed by schematic page, of all parts used in the design with their
part references, part names and libraries.
o Then, the Create Netlist Tool will create a netlist and move the design into Orcad Layout.

[3]BOARD DESIGN WITH ORCAD LAYOUT

Using Orcad Capture the designer has created an Orcad Layout-compatible netlist that includes critical design rules such as component locations, net spacing criteria, component group information, net widths, and routing layers. Orcad Layout will use these preset design rules to guide logical placement and routing.
The Orcad Unison AutoECO process allows the designer to create a new board layout by combining the netlist from Orcad Capture with an Orcad Layout board template file. The template file may contain physical properties such as the outline for the board, routing and placement strategies, number of layers, grids, and other information that Layout will use in the board design.

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During the AutoECO process, if a footprint listed in the netlist is not found in the Orcad Layout footprint libraries, a
dialog box will appear allowing the designer to select an appropriate footprint for that component. If no problems
are encountered during AutoECO, the designer can begin placing components and routing the design.
Orcad Layout's manual placement tools provide complete control of the component placement process, allowing
components to be placed individually or in groups. The Queue For Placement command makes a component or
group of components available for placement based on a set of criteria (reference designator, footprint name, first
letters with wildcards, etc.). The designer can then place the components individually using the Select Next command.
Functionally related components can be assigned to groups in the circuit schematic while in Orcad Capture. Then,
when the group number (as assigned in the schematic) is specified in the Orcad Layout's Component Selection
Criteria dialog box, the components assigned to the group snap to the cursor for placement.
When all components are placed, the designer can check placement using the DRC check for Placement Spacing
Violations, review the routing density in the density graphics window, and inspect the placement information in
Orcad Layout's Statistics spreadsheet. The Placement Spacing Violations feature looks for component-to-component spacing violations and other placement errors, such as components that violate height restrictions, insertion outlines, or grid restrictions. Any problem found by Placement Spacing Violations is marked with a circle.
The density graph displays a graphical representation of the component and connection density of the board. Using colors ranging from blue and green (acceptable density) to pink and red (very dense), the density graph represents the degree of difficulty that will be faced in routing the board.
3
The Statistics spreadsheet shows the percentage and number of components placed, how many were placed off the board, how many were unplaced, and how many were placed in clusters.
In addition, Orcad Layout has the ability to communicate interactively with Orcad Capture using intertool communication. Intertool communication supports cross-probing to facilitate design analysis. If a part is selected on the schematic in Orcad Capture, the corresponding component is highlighted in Orcad Layout, and vice versa. Using cross-probing, the designer can select important parts on the schematic and confirm their placement in the board design. The designer can also back annotate board data to Orcad Capture from Orcad Layout.
After components are placed, the board must be routed to form the electrical connections between components.
With Orcad Layout, the board can be routed manually or automatically using Layout's interactive and automatic
routing tools. Using manual routing, the designer guides the routing process and manually routes each track.
Routing is then optimized using a variety of manual routing commands. The Minimize Connections command, for
example, finds the shortest connection possible for each connection that has not yet been routed. If nothing is
selected, it reconnects the entire board. If a net is selected, it will minimize the connection for just that net.
In interactive routing, the designer still controls the routing of individual tracks, but can also take advantage of
Layout's automatic routing technologies, such as push-and-shove, which moves tracks to make space for the track
currently being routing. Layout's gridded autorouter has two key features: sweep technology, which allows the designer to specify the directional emphasis for routing different boards, and shove technology, which minimizes vias and allows dense autorouting. The autorouter initiates a series of routing passes that systematically routes an entire board.
Orcad Layout's autorouter can be interrupted at any time to manage and control the routing process. The designer
can autoroute a single track, a selected area of the board, a group of nets, or the entire board. In addition, Orcad
Layout provides a seamless interface to the sophisticated SPECCTRA autorouter, allowing easy routing of more dense designs.

As a rule of thumb, Orcad Layout's gridded autorouter can be used if the design is a low density design – more than 0.30 square inches of board space per equivalent IC – it lends itself to the orthogonal routing of a gridded router, and it does not have BGA or fine-pitch parts.
The SPECCTRA shape-based autorouter should be used if the design is a higher density design – less than 0.30 square inches of board space per equivalent IC – or is a design that would benefit from diagonal routing, or has BGA or fine-pitch parts.

[4]AUTOROUTING WITH SPECCTRA

If the design is very dense and autorouting is required, the SPECCTRA autorouter can be launched from within Orcad Layout. While SPECCTRA is active, the board design session in Orcad Layout is suspended.
SPECCTRA autorouting is designed to handle high-speed, high-density PCB systems that require complex design rules.
It employs powerful, shape-based algorithms to make the most efficient use of the routing area.
SPECCTRA routes designs by modeling objects (such as pins, pads, wires, and vias) as true shapes. Each shape on each layer inherits its own set of design rules. The autorouter attempts to wire all connections by allowing wiring
conflicts (crossing and clearance violations) during the first routing pass. These conflicts are eliminated during
subsequent routing passes. After each routing pass, conflicts are marked graphically with a conflict box (clearance
violation) or a diamond (crossover violation).
During the first routing pass, the autorouter allows conflicts in order to route every connection. Each subsequent
routing pass modifies the routed wiring using rip-up and retry methods that continuously improve overall results.
The cost for creating conflicts increases with each subsequent pass.
During the first five routing passes, all connections are ripped up and rerouted. After the first five routing passes,
the routing strategy changes, and only wires involved in conflicts are ripped up and rerouted. Wires that are not
involved in conflicts are ignored during this phase.
The goal of the sixth and all subsequent routing passes is to eliminate all remaining conflicts and achieve 100
percent completion. As many as 100 or more routing passes may be required to eliminate all conflicts in large
difficult designs.
However, if the autorouter encounters a situation where the reduction ratio over multiple passes is small and more
than 50 failures remain, it automatically removes the "gridlocked" wires and continues. Orcad Layout's interactive
routing tools can be used to manually route these connections.
4
All routing failures are monitored and recorded in a status file. A failure occurs when the autorouter is unable to
find a new path for a connection. During pass one, failures are unroutes. After pass one, failures can consist of
unroutes and wires that cannot be rerouted with a different path.
When SPECCTRA autorouting is complete and the routing information is ready to be returned to Orcad Layout, the
designer need only close SPECCTRA. The routing information will be automatically read back into Orcad Layout and the routing will appear on the board design.

POSTPROCESSING WITH ORCAD LAYOUT

In Orcad Layout, all output settings are stored in a spreadsheet that can be saved and revised. This Post Process
spreadsheet allows the designer to preview and select the proper output for each layer before creating the actual
output files.
The designer can give layer-by-layer instructions for writing to Gerber files, DXF files, or hardcopy devices. Layout

produces more than twenty standard reports – including fabrication drawings, assembly drawings, and pick-andplace reports – and can accommodate designer-customized reports.
To generate Gerber, DXF or hardcopy output files, the designer uses the Run Post Processor command. Output files are automatically created for each layer that was batch-enabled while previewing the outputs. The format
generated is the format selected while setting the Post Process Settings. The file extension used for each output file is appropriate for the type of output.
GerbTool, which is supplied with Orcad Layout, allows the designer to view output Gerber files in order to verify
that they are exactly what as expected before they are sent out for fabrication. GerbTool reads and writes all
standard Gerber formats. In addition it features automatic tear-dropping, panelization, venting and thieving, and
removal of unused pads and silkscreen on pads. GerbTool also allows the designer to perform other prep work to
ensure that files will be exactly what the board fabrication shop requires. Orcad provides industry standard manufacturing formats such as IPC-356 and GenCAD. As formats evolve and new formats are defined, software
updates reflecting these changes are placed on our web site for free download and immediate use.

[5]CONCLUSION

Most problems in PCB designs can be traced to incorrect component information or poor communication between
designers and layout engineers. Specifying an obsolete component or one that has an unexpectedly long lead time
can result in expensive rework. Even a simple communication error can trigger an extra board turn and delay a
project significantly. This can happen, for example, when a designer changes an IC package or the wattage of a
resistor without changing the corresponding PCB footprint and company part number.
Such errors are easy to make, especially when design and layout teams use loosely connected tools and communicate via email messages and handwritten notes. If discovered early in the design process, these errors can be easily avoided. If discovered after the board has been fabricated, assembled or shipped in a product, problems may be tens or hundreds of times more expensive to correct. The tight integration of the Orcad Unison Suite of PCB tools eliminates these sources of errors and allows the designer to move board designs from creation to manufacturing with more complete information every step of the way.
5

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